True Circuits, Inc.

PLL and DLL Hard Macros

True Circuits' complete family of standardized, silicon-proven, low-jitter PLL and DLL hard macros spans nearly all performance points and features typically requested by ASIC, FPGA and SoC designers. Using robust state-of-the-art circuits, a methodical and proven design strategy, and a close association with the world's leading fabs, IDMs and design services companies, True Circuits is able to quickly and reliably create new and innovative designs in a variety of advanced process technologies.

True Circuits' leading clock generator, spread spectrum, low bandwidth, high resolution and deskew PLLs support wide operating frequency ranges and multiplication factors over which they deliver optimal performance, eliminating the need for PLL generators that attempt to optimize performance at a single operating point. The clock generator PLL is available with multi-phase outputs and 4 bits of precise factional-N control. The high resolution PLL provides frequency modulation and very high frequency resolution with over 16 bits of control and very low long-term jitter. All PLLs are available in small sizes for easier integration.

True Circuits' DLLs delay a set of signals by precise and adjustable fractions of a reference clock cycle independent of voltage and temperature. These DLLs have flexible form factors for easier integration and are ideal for high-speed DDR and other interface applications.

True Circuits' high-quality, low-jitter, silicon-proven timing hard macros are available for immediate delivery in a range of frequencies, multiplication factors, sizes and functions in TSMC, UMC, CHRT and Common Platform processes from 180nm to 40nm.

Features & Benefits

- Clock Generator, Spread Spectrum, Low Bandwidth, High Resolution, and Deskew PLLs
- High-speed DLLs
- Support latest DDR, SerDes and video standards
- Low-jitter and very process tolerant
- Large multiplication factors (1-4096)
- Wide output frequency ranges
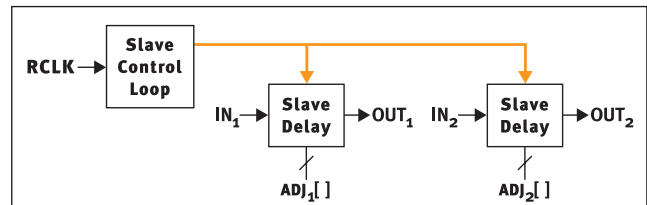- Small sizes and flexible form factors
- Pin programmable

Clock Generator, Spread Spectrum, Low Bandwidth and High Resolution PLLs
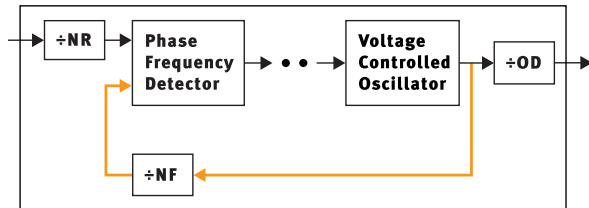
Deskew PLL
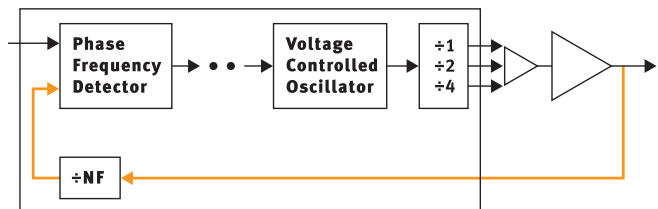
DDR DLL

Technical Specs

- Available in TSMC, UMC, CHRT and Common Platform processes from 180nm to 40nm
- GDSII and LVS Spice netlists
- Behavioral, synthesis and LEF models
- Extensive user documentation
- Integration support to ensure successful tape outs

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